rocketick

RocketSim™

Give your simulation a boost

Fast and Seamless Verilog Co-Simulator

Compatible with leading simulators:

cadence™ SYNOPSYS® Mentor Graphics®

RocketSim™ solves functional verification bottlenecks by complementing simulators with a Multicore Processor based acceleration solution that offers 5-10X faster simulations for complex designs

Functional Verification Bottlenecks

Functional verification is a severe bottleneck in chip design projects. The ever-growing chip density and complexity impacts the time it takes simulators to complete each run. When each simulation takes days to complete, either the product's time-to-market is affected or in some cases teams tape-out early with less confidence.

Complementing Simulators with a Multicore Processor based Co-Simulator

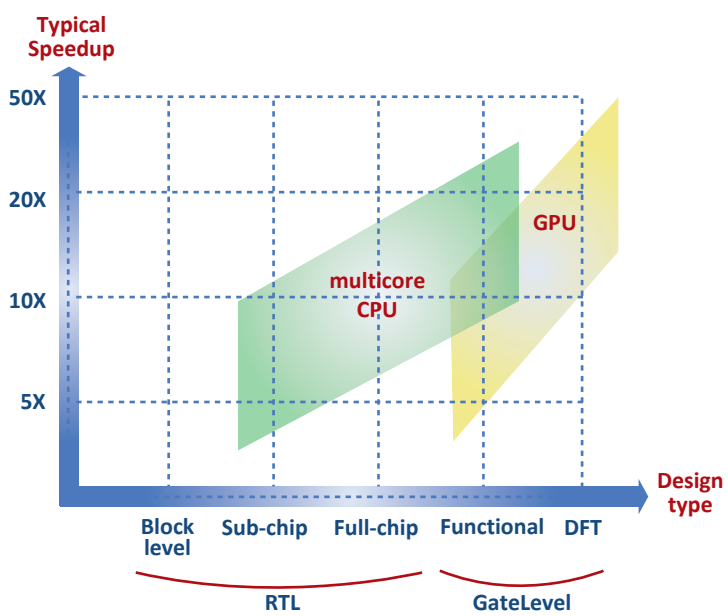
RocketSim™ solves the simulator's bottleneck challenge by offloading most time-consuming calculations to an ultra-fast multithreaded engine. Unlike hardware based accelerators, RocketSim™ works from within the familiar simulator environment and runs alongside the existing test bench, eliminating ramp-up time while providing 4-state bit-precise results.

Supports Large Designs with Full Debug Visibility

RocketSim™ supports large and complex designs (over one billion gates), while offering full visibility of your design. RocketSim™ enables expending the verification scope to include larger designs and more complex tests.

Main Features

- Software-based solution installed on standard servers
- Accelerates leading simulators (Incisive, VCS and ModelSim)
- Rapid Compilation
- Full debug visibility
- Direct dump of FSDB/SST2
- Over one billion logic gate capacity
- Compliant with Verilog IEEE 1364-2001, 1364-2005, VHDL, System Verilog, OVM, VMM and UVM
- PLI/VPI compliant interface
- Runs alongside the test-bench
- Full support for 4-state logic
- Highly scalable (multiple GPUs, multicore)
- Quick ramp-up



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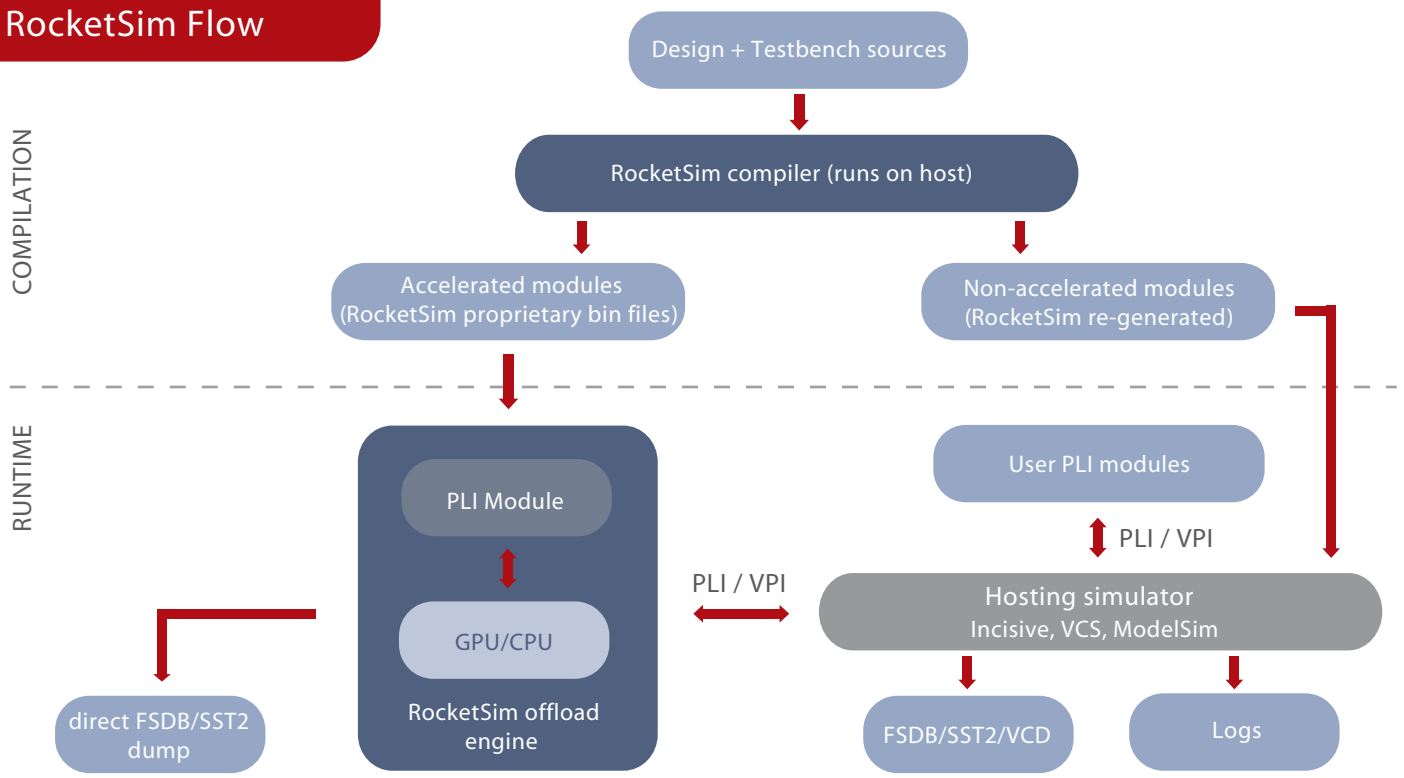
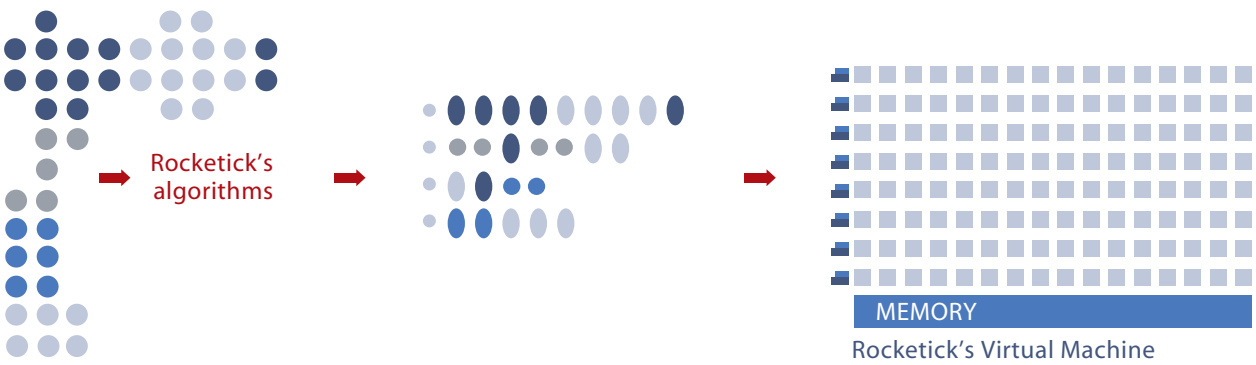
RocketSim Flow



During compilation, RocketSim's compiler runs on the host machine, separating the design from the testbench. During runtime, the design is accelerated while the testbench runs on the host simulator. To achieve a faster simulation, a large portion of the logic is offloaded to RocketSim's acceleration engine, running on multicore hardware (Intel's XEON CPUs or Nvidia GPUs) where state synchronization is done via PLI .

Breaking the Dependency Barrier

Complex dependency graph



Logical simulators run highly complex calculations with extensive dependencies, limiting their ability to conduct parallel processing. RocketSim™ breaks this dependency barrier - it analyses the dependencies and translates most of them into independent threads that can run in parallel on a multicore processors, which offers massive parallel computing.

Investors

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